REMARKS/ARGUMENTS

Claims 1-20 remain pending. Claims 1-4, 8-11, and 15-19 have been amended.

Applicant amended claims 1-4, 8-11, and 15-19 to correct the informalities and point out the subject matter which applicant regards as the invention. Thus, the objection of above claims can be traversed.

Applicants respectfully requests reconsideration in light of the following remarks.

CLAIM REJECTIONS

Rejection of Claims 1-3, 5-6, 8-10, 12-13, 15, 17, and 19 under 35 U.S.C. 102(b)

Claim 1-3, 5-6, 8-10, 12-13, 15, 17, and 19, in so far as understood, rejected under 35 U.S.C. 102(b) as being anticipated by Guttag et al. 5,493,646. Applicant respectfully submits that such rejection is improper for the following reasons:

Guttag et al. disclose a data processor with a transparency detection data transfer controller transfers data from a block of source addresses to a block of destination addresses. The applicant's invention is to provide a system chip with a central processing unit, an external temporary data segment, coupled to the control chip with a memory bus, and a memory interface control circuit for transforming an internal data accessing address and corresponding to the external temporary data segment, so that the CPU could directly access data from the external temporary data segment. The applicant's invention redirects the data accessing request of accessing flow control parameters and numerical arithmetic to the

external memory in accompanied with suspending/reviving CPU clock, which is not disclosed by Guttag et al.. The processing unit will be unconscious of these redirecting activities due to CPU clock was suspended during redirecting periods. As the result, the internal memory can be decreased or replaced by the external temporary data segment.

Moreover, the first time cycle and the second time cycle of the applicant's invention belong to the processor and memory respectively, wherein the second time cycle is about that other device is accessing the memory more particularly. Guttag et al discloses 3 different block-write mechanisms supported by the transfer controller: "8.times.", "4.times.", and "simulated". The system hardware determines the block-write mechanism at the time that the block-write begins. This allows software to use block-write without regard to what type of block-write the system uses or whether or not the addressed memory supports it (column 76, lines 41-47). The block-write mode used by transfer controller is selected by the value input on the BS[1:0] pins of multiprocessor integrated circuit by external circuitry (column 76, lines 52-54). Thus, the block-write modes are not the operating cycles and controlled by the multiprocessor integrated circuit, which is different from the first and second time cycle that belong to the processor and memory respectively of the applicant's invention.

Thus this rejection is respectfully traversed on the basis that Guttag et al. do not teach the applicant's invention.

Rejection of Claims 7, 14, and 20 under 35 U.S.C. 103(a)

Claim 7, 14, and 20, in so far as understood, rejected under 35 U.S.C. 103(a) as being unpatentable over Guttag et al. and further in view of Ripley et al.. Applicant respectfully submits that such rejection is improper for the following reasons:

Ripley et al. disclose a method for verifying the integrity of a media key block (MKB) by storing validation data in a cutting area of a medium, such as a DVD-R or a DVD-RW. As the description above, Guttag et al. do not teach the applicant's invention that redirects the data accessing request of accessing flow control parameters and numerical arithmetic to the external memory in accompanied with suspending/reviving CPU clock. And the objects of Guttag et al. and Ripley et al. are different that the object of Ripley et al. is to verifying the validation data of a medium and the object of Guttag et al. is to specifiès the transparency data. The citations, Guttag et al. and Ripley et al., are not able to be combined and Ripley et al. do not disclose the applicant's invention that provide a system chip to improve the design of temporary storage and with reducing temporary memory, and further provides a system chip with the reducing area and manufacture cost.

Rejection of Claims 4, 11, and 18 under 35 U.S.C. 103(a)

Claim 4, 11, and 18, in so far as understood, rejected under 35 U.S.C. 103(a) as being unpatentable over Guttag et al. and further in view of Wise et al.. Applicant respectfully submits that such rejection is improper for the following reasons:

Wise et al. disclose a method of accessing a memory having a plurality of memory locations comprising static RAM cells. An object of Wise et al. is to provide a memory and method of accessing a memory in which accessing may be carried out to effect a data transfer at each clock cycle while permitting more than one clock cycle for an equating operation for the bit lines, wherein when using memories comprising static RAM cells it is normally necessary to equate bit lines prior to reading data from the cell (column 1, lines 26-28). .Thus the equating operation is before the reading and writing operation. The applicant's invention discloses a method for suspending a first time clock when sending an access request signal

and reviving the first time clock when receiving an acknowledgement signal, wherein the suspending is to resolves the problem of memory accessed by central processing unit and other device at the same time. Thus the suspending is not equal to the equating.

As the description above, Guttag et al. do not teach the applicant's invention that redirects the data accessing request of accessing flow control parameters and numerical arithmetic to the external memory in accompanied with suspending/reviving CPU clock. The combination of the citations, Guttag et al. and Wise et al., is not able to provide a system chip with the reducing area and manufacture cost that improves the design of temporary storage, reduces temporary memory, and is capable of accessing data from an external temporary data segment of an external memory chip, in the prior art. The combination of Guttag et al. and Wise et al. don't teach the result which is described in the applicant's invention.

CONCLUSION

In the light of the above remarks, Applicant respectfully submits those pending Claims 1-20 as currently presented are in condition for allowance. Applicant has thoroughly reviewed that art cited but relied upon by the Examiner. Applicant has concluded that this cited reference do not affect the patentability of these claims as currently presented. Accordingly, reconsideration is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,
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AMENDMENTS TO THE DRAWINGS:

The attached sheet of drawings includes changes to Fig. 2A and Fig. 2B. This sheet, which includes Fig. 2A and Fig. 2B, replaces the original sheet including Fig. 2A and Fig. 2B. In Fig. 2A and Fig. 2B, previously omitted labels "Memory Chip", "Temporary Storage", "CPU", "Control Circuit", and "Necessary Circuit" have been added.

Attachment: Replacement Sheet